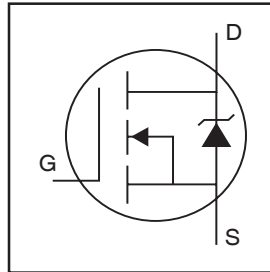


**AUTOMOTIVE MOSFET**

**IRLR3105PbF**  
**IRLU3105PbF**  
HEXFET® Power MOSFET

**Features**

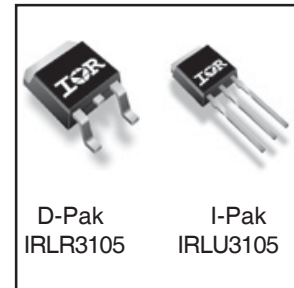
- Logic-Level Gate Drive
- Advanced Process Technology
- Ultra Low On-Resistance
- 175°C Operating Temperature
- Fast Switching
- Repetitive Avalanche Allowed up to Tjmax
- Lead-Free



$V_{DSS} = 55V$
$R_{DS(on)} = 0.037\Omega$
$I_D = 25A$

**Description**

Specifically designed for Automotive applications, this HEXFET® Power MOSFET utilizes the latest processing techniques to achieve extremely low on-resistance per silicon area. Additional features of this design are a 175°C junction operating temperature, fast switching speed and improved repetitive avalanche rating. These features combine to make this design an extremely efficient and reliable device for use in Automotive applications and a wide variety of other applications.



The D-Pak is designed for surface mounting using vapor phase, infrared, or wave soldering techniques. The straight lead version (IRLU series) is for through-hole mounting applications. Power dissipation levels up to 1.5 watts are possible in typical surface mount applications.

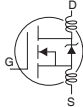
**Absolute Maximum Ratings**

	Parameter	Max.	Units
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	25	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	18	
$I_{DM}$	Pulsed Drain Current ①	100	
$P_D @ T_C = 25^\circ C$	Power Dissipation	57	W
	Linear Derating Factor	0.38	W/°C
$V_{GS}$	Gate-to-Source Voltage	$\pm 16$	V
$E_{AS}$	Single Pulse Avalanche Energy ②	61	mJ
$E_{AS} (tested)$	Single Pulse Avalanche Energy Tested Value ②	94	
$I_{AR}$	Avalanche Current ①	See Fig.12a, 12b, 15, 16	A
$E_{AR}$	Repetitive Avalanche Energy ③		mJ
dv/dt	Peak Diode Recovery dv/dt ③	3.4	V/ns
$T_J$	Operating Junction and	-55 to + 175	°C
$T_{STG}$	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case )	

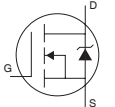
**Thermal Resistance**

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	2.65	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB mount)*	—	50	
$R_{\theta JA}$	Junction-to-Ambient	—	110	

## Electrical Characteristics @ T<sub>J</sub> = 25°C (unless otherwise specified)

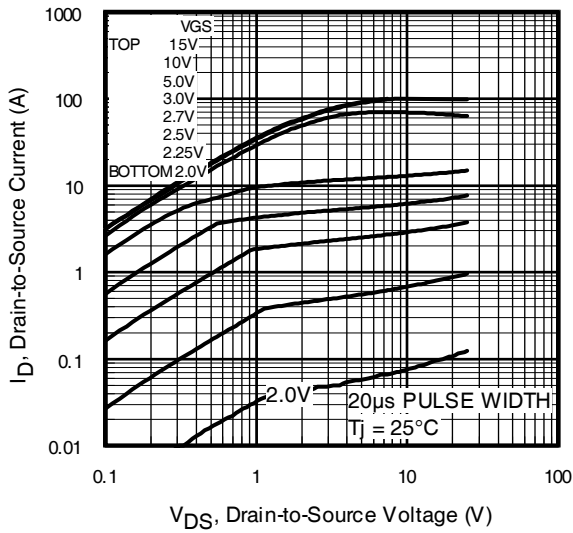
	Parameter	Min.	Typ.	Max.	Units	Conditions
V <sub>(BR)DSS</sub>	Drain-to-Source Breakdown Voltage	55	—	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA
ΔV <sub>(BR)DSS</sub> /ΔT <sub>J</sub>	Breakdown Voltage Temp. Coefficient	—	0.056	—	V/°C	Reference to 25°C, I <sub>D</sub> = 1mA
R <sub>DS(on)</sub>	Static Drain-to-Source On-Resistance	—	30	37	mΩ	V <sub>GS</sub> = 10V, I <sub>D</sub> = 15A ④
		—	35	43		V <sub>GS</sub> = 5.0V, I <sub>D</sub> = 13A ④
V <sub>GS(th)</sub>	Gate Threshold Voltage	1.0	—	3.0	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA
g <sub>fs</sub>	Forward Transconductance	15	—	—	S	V <sub>DS</sub> = 25V, I <sub>D</sub> = 15A④
I <sub>DSS</sub>	Drain-to-Source Leakage Current	—	—	20	μA	V <sub>DS</sub> = 55V, V <sub>GS</sub> = 0V
		—	—	250		V <sub>DS</sub> = 44V, V <sub>GS</sub> = 0V, T <sub>J</sub> = 150°C
I <sub>GSS</sub>	Gate-to-Source Forward Leakage	—	—	200	nA	V <sub>GS</sub> = 16V
	Gate-to-Source Reverse Leakage	—	—	-200		V <sub>GS</sub> = -16V
Q <sub>g</sub>	Total Gate Charge	—	—	20	nC	I <sub>D</sub> = 15A
Q <sub>gs</sub>	Gate-to-Source Charge	—	—	5.6		V <sub>DS</sub> = 44V
Q <sub>gd</sub>	Gate-to-Drain ("Miller") Charge	—	—	9.0		V <sub>GS</sub> = 5.0V, See Fig. 6 and 13
t <sub>d(on)</sub>	Turn-On Delay Time	—	8.0	—		V <sub>DD</sub> = 28V
t <sub>r</sub>	Rise Time	—	57	—		I <sub>D</sub> = 15A
t <sub>d(off)</sub>	Turn-Off Delay Time	—	25	—		R <sub>G</sub> = 24Ω
t <sub>f</sub>	Fall Time	—	37	—		V <sub>GS</sub> = 5.0V, See Fig. 10 ④
L <sub>D</sub>	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact
L <sub>S</sub>	Internal Source Inductance②	—	7.5	—		
C <sub>iss</sub>	Input Capacitance	—	710	—	pF	V <sub>GS</sub> = 0V
C <sub>oss</sub>	Output Capacitance	—	150	—		V <sub>DS</sub> = 25V
C <sub>rss</sub>	Reverse Transfer Capacitance	—	28	—		f = 1.0MHz, See Fig. 5
C <sub>oss</sub>	Output Capacitance	—	890	—		V <sub>GS</sub> = 0V, V <sub>DS</sub> = 1.0V, f = 1.0MHz
C <sub>oss</sub>	Output Capacitance	—	110	—		V <sub>GS</sub> = 0V, V <sub>DS</sub> = 44V, f = 1.0MHz
C <sub>oss eff.</sub>	Effective Output Capacitance ③	—	210	—		V <sub>GS</sub> = 0V, V <sub>DS</sub> = 0V to 44V

## Source-Drain Ratings and Characteristics

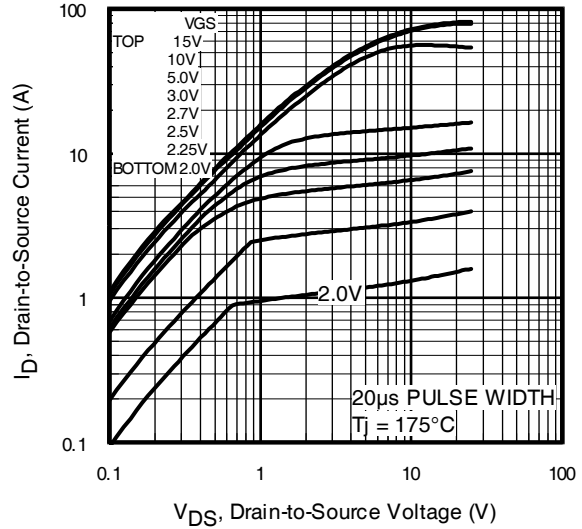
	Parameter	Min.	Typ.	Max.	Units	Conditions
I <sub>S</sub>	Continuous Source Current (Body Diode)	—	—	25	A	MOSFET symbol showing the integral reverse p-n junction diode.
I <sub>SM</sub>	Pulsed Source Current (Body Diode) ①	—	—	100		
V <sub>SD</sub>	Diode Forward Voltage	—	—	1.3	V	T <sub>J</sub> = 25°C, I <sub>S</sub> = 15A, V <sub>GS</sub> = 0V ④
t <sub>rr</sub>	Reverse Recovery Time	—	52	78	ns	T <sub>J</sub> = 25°C, I <sub>F</sub> = 15A, V <sub>DD</sub> = 28V
Q <sub>rr</sub>	Reverse Recovery Charge	—	82	120	nC	di/dt = 100A/μs ④
t <sub>on</sub>	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L <sub>S</sub> +L <sub>D</sub> )				

\* When mounted on 1" square PCB (FR-4 or G-10 Material) .  
For recommended footprint and soldering techniques refer to application note #AN-994

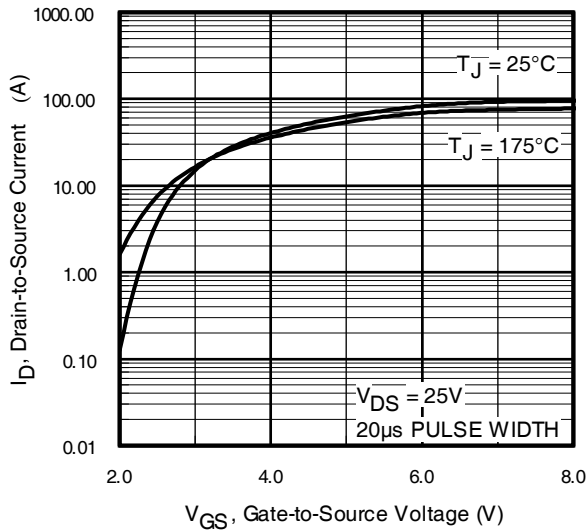
Notes ① through ④ are on page 11



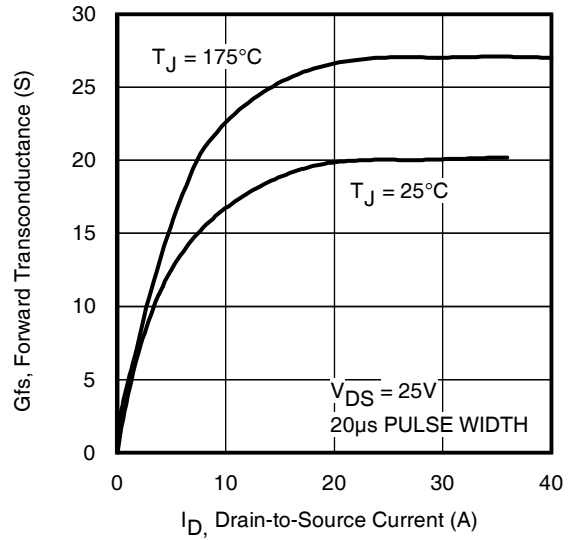
**Fig 1.** Typical Output Characteristics



**Fig 2.** Typical Output Characteristics

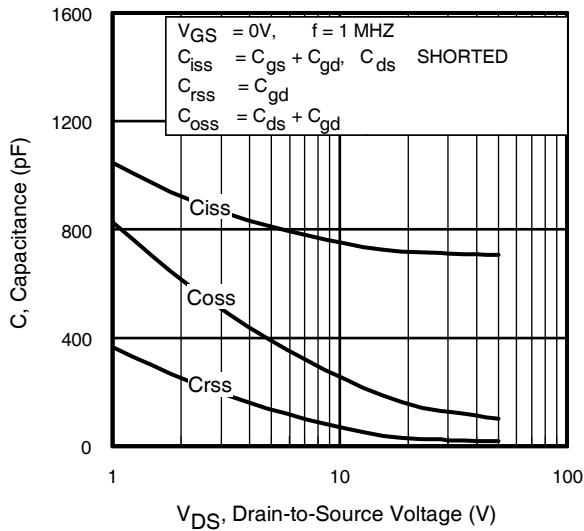


**Fig 3.** Typical Transfer Characteristics

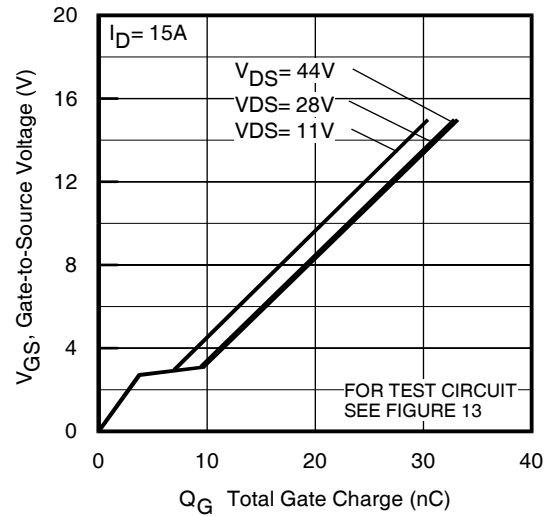


**Fig 4.** Typical Forward Transconductance Vs. Drain Current

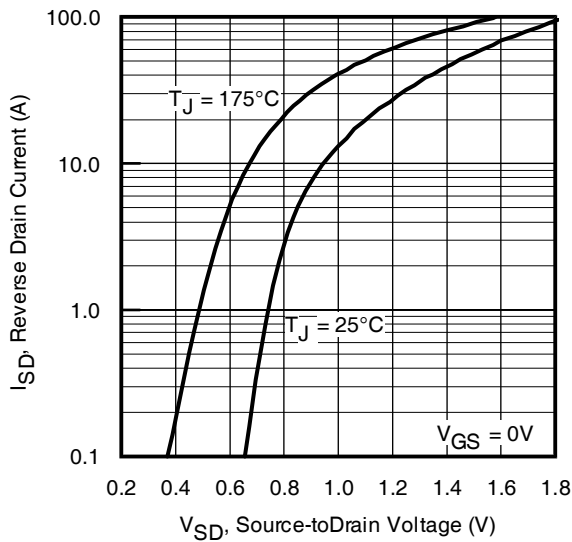
# IRLR/U3105PbF



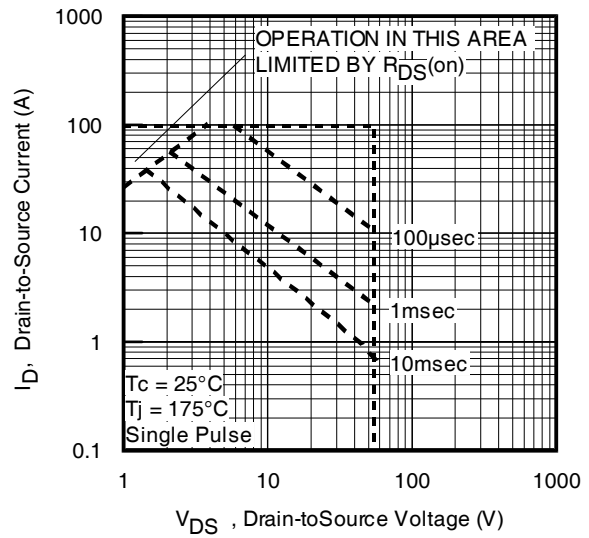
**Fig 5.** Typical Capacitance Vs. Drain-to-Source Voltage



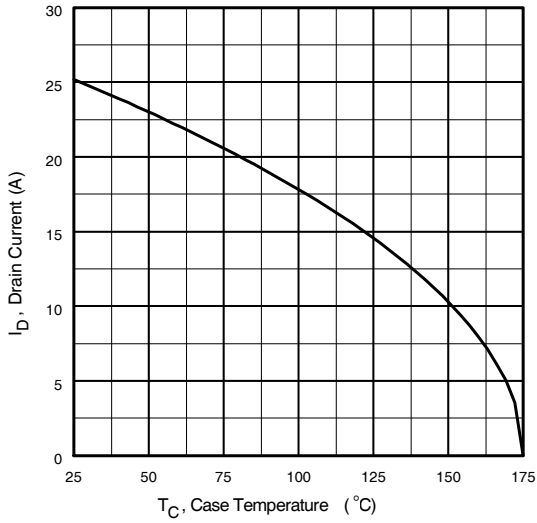
**Fig 6.** Typical Gate Charge Vs. Gate-to-Source Voltage



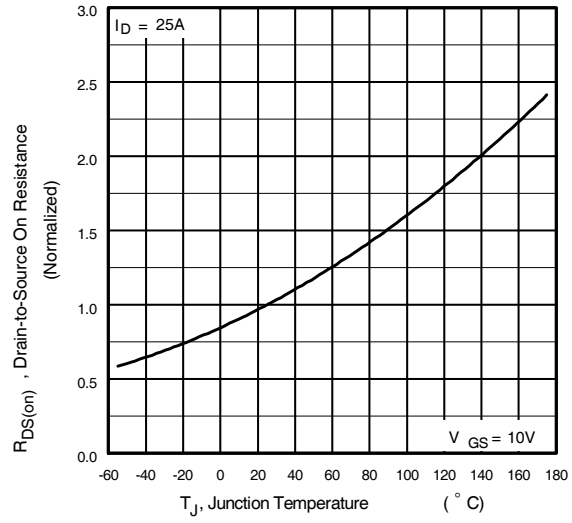
**Fig 7.** Typical Source-Drain Diode Forward Voltage



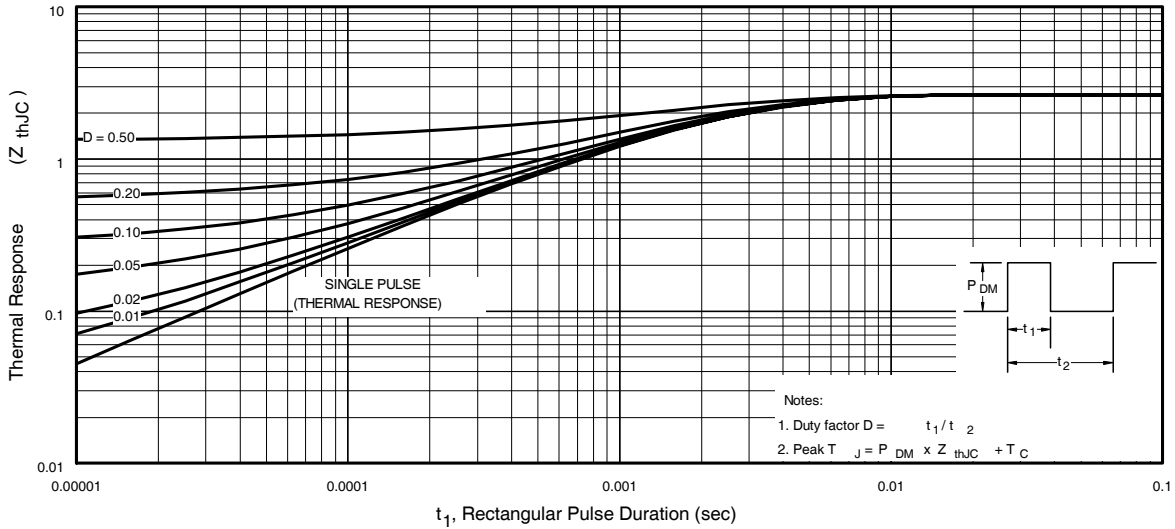
**Fig 8.** Maximum Safe Operating Area



**Fig 9.** Maximum Drain Current Vs. Case Temperature

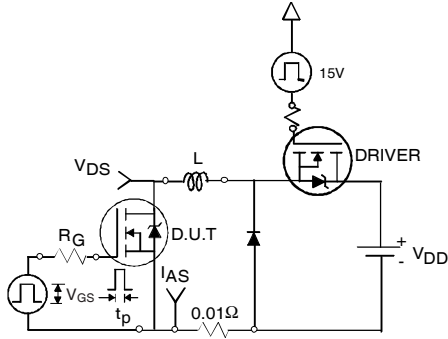


**Fig 10.** Normalized On-Resistance Vs. Temperature



**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case

# IRLR/U3105PbF



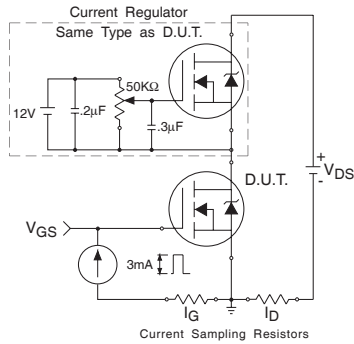
**Fig 12a.** Unclamped Inductive Test Circuit



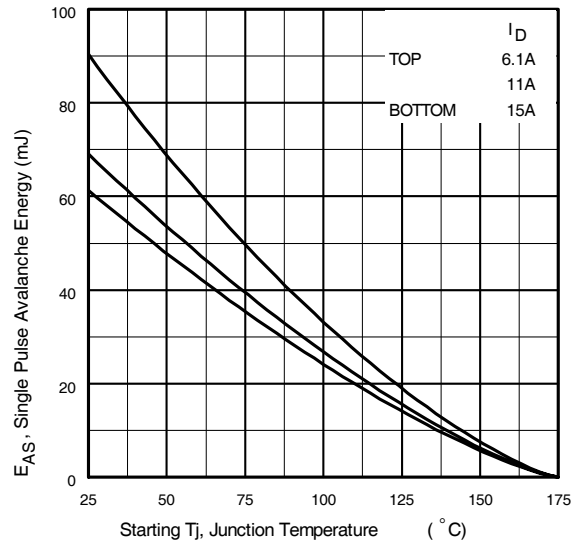
**Fig 12b.** Unclamped Inductive Waveforms



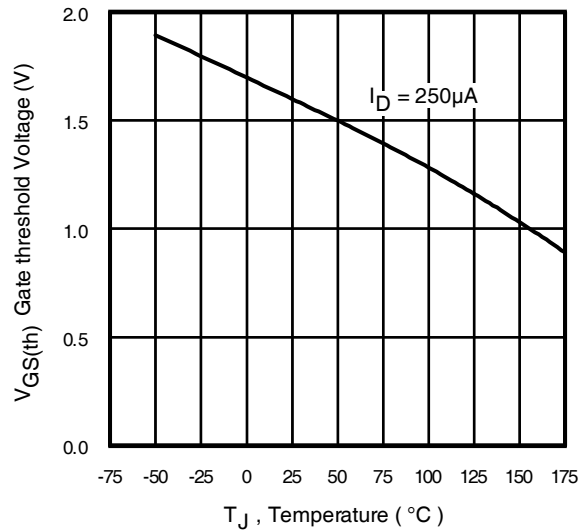
**Fig 13a.** Basic Gate Charge Waveform



**Fig 13b.** Gate Charge Test Circuit



**Fig 12c.** Maximum Avalanche Energy Vs. Drain Current



**Fig 14.** Threshold Voltage Vs. Temperature

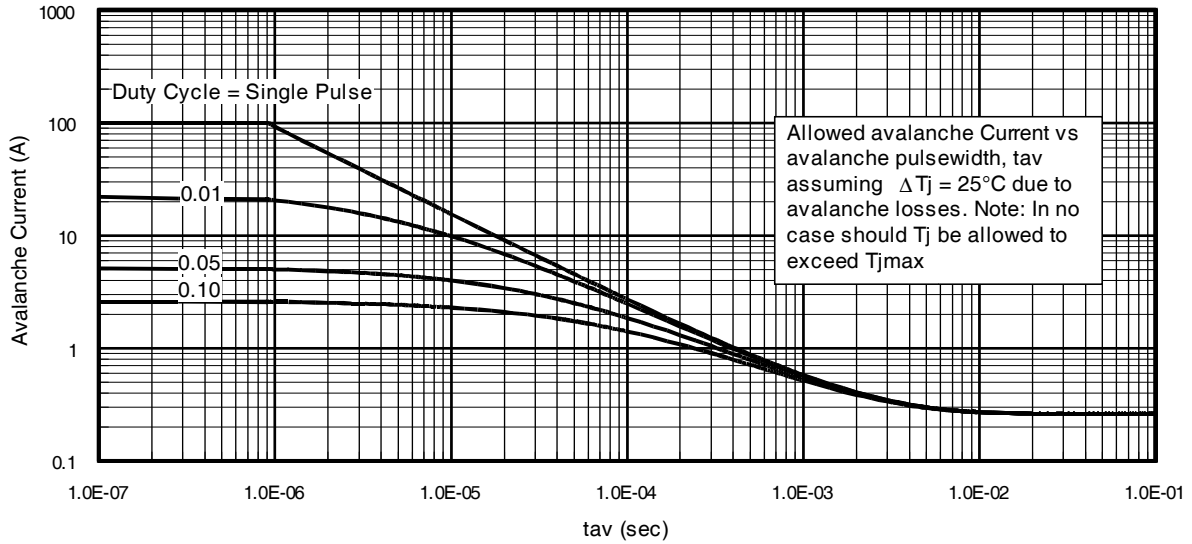


Fig 15. Typical Avalanche Current Vs. Pulsewidth

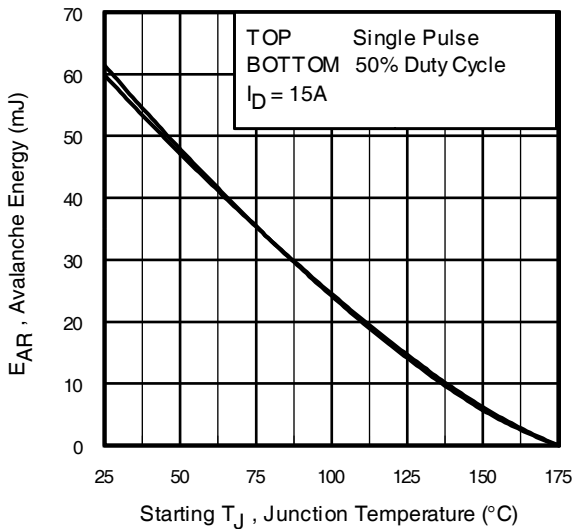


Fig 16. Maximum Avalanche Energy Vs. Temperature

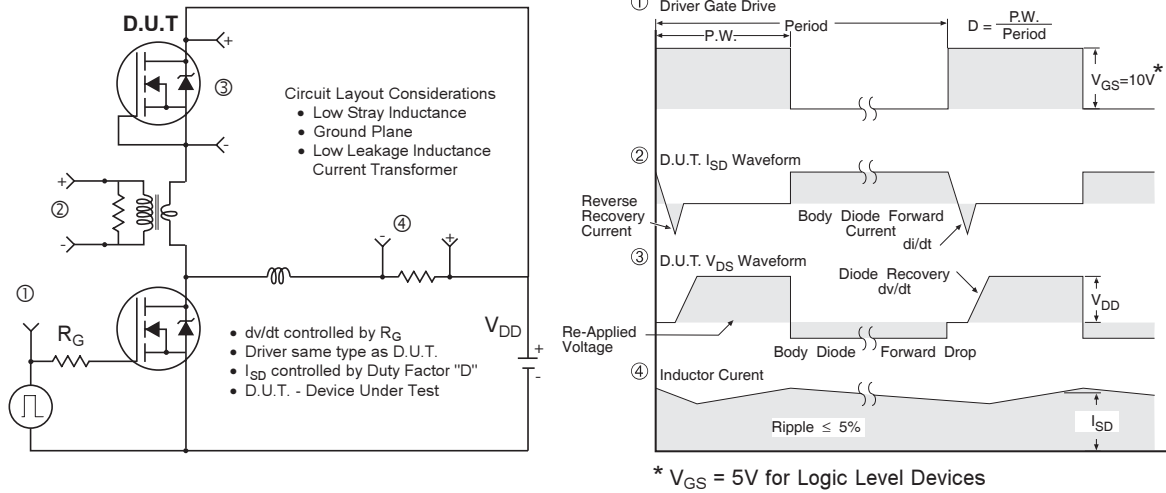
**Notes on Repetitive Avalanche Curves , Figures 15, 16:**  
(For further info, see AN-1005 at [www.irf.com](http://www.irf.com))

1. Avalanche failures assumption:  
Purely a thermal phenomenon and failure occurs at a temperature far in excess of  $T_{jmax}$ . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as  $T_{jmax}$  is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 12a, 12b.
4.  $P_{D(ave)}$  = Average power dissipation per single avalanche pulse.
5.  $BV$  = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6.  $I_{av}$  = Allowable avalanche current.
7.  $\Delta T$  = Allowable rise in junction temperature, not to exceed  $T_{jmax}$  (assumed as 25°C in Figure 15, 16).  
 $t_{av}$  = Average time in avalanche.  
 $D$  = Duty cycle in avalanche =  $t_{av} \cdot f$   
 $Z_{thJC}(D, t_{av})$  = Transient thermal resistance, see figure 11)

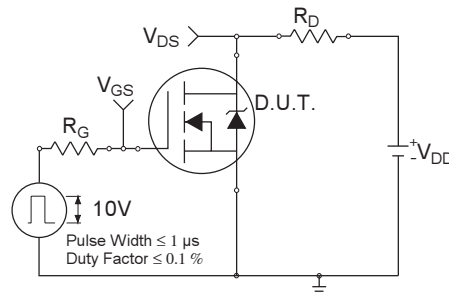
$$P_{D(ave)} = 1/2 ( 1.3 \cdot BV \cdot I_{av} ) = \Delta T / Z_{thJC}$$

$$I_{av} = 2\Delta T / [ 1.3 \cdot BV \cdot Z_{th} ]$$

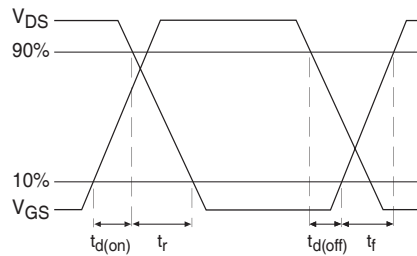
$$E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$$



**Fig 17. Peak Diode Recovery  $dv/dt$  Test Circuit for N-Channel HEXFET® Power MOSFETs**



**Fig 18a. Switching Time Test Circuit**

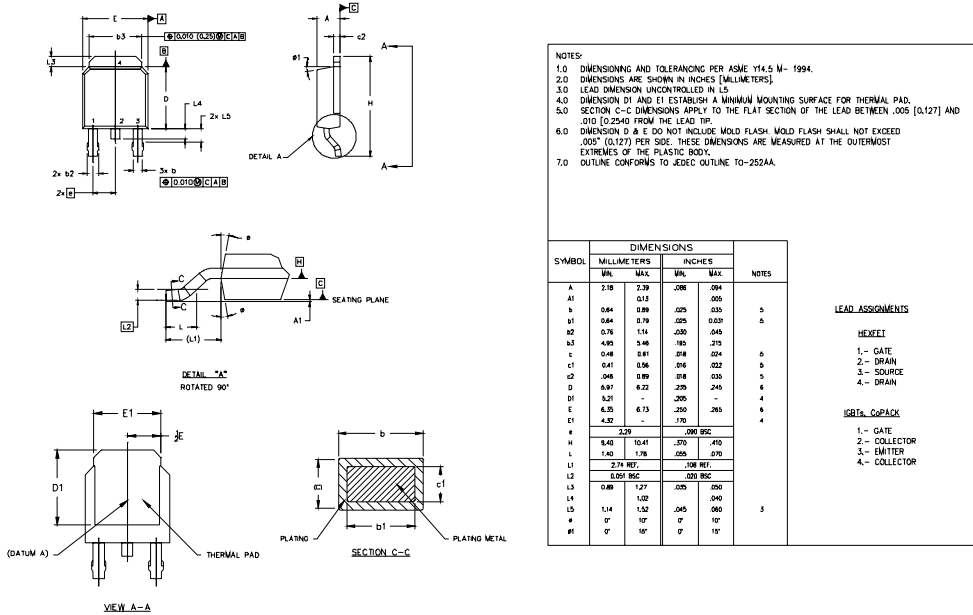


**Fig 18b. Switching Time Waveforms**



## D-Pak (TO-252AA) Package Outline

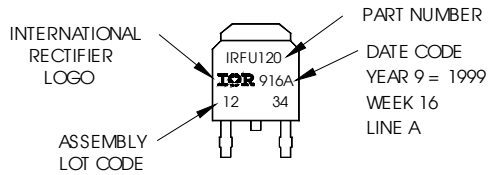
Dimensions are shown in millimeters (inches)



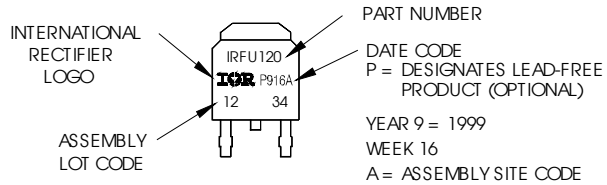
## D-Pak (TO-252AA) Part Marking Information

EXAMPLE: THIS IS AN IRFR120  
WITH ASSEMBLY  
LOT CODE 1234  
ASSEMBLED ON WW 16, 1999  
IN THE ASSEMBLY LINE "A"

Note: "P" in assembly line position  
indicates "Lead-Free"



OR

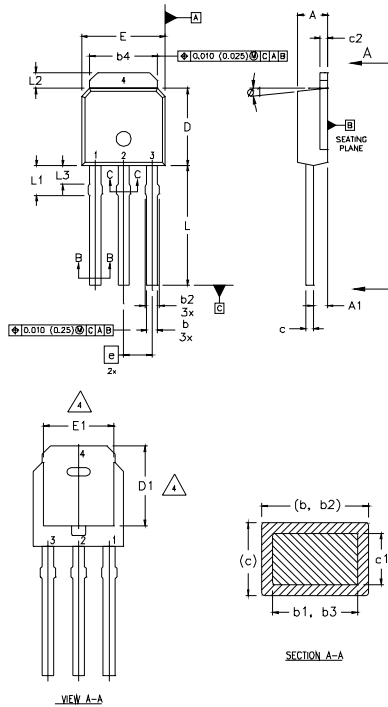


# IRLR/U3105PbF

International  
**IR** Rectifier

## I-Pak (TO-251AA) Package Outline

Dimensions are shown in millimeters (inches)



- NOTES:
- 1 DIMENSIONING AND TOLERANCING PER ASME Y14.5 M- 1994.
  - 2 DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
  - 3 DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
  - 4 THERMAL PAD CONTOUR OPTION WITHIN DIMENSION b4, L2, E1 & D1.
  - 5 LEAD DIMENSION UNCONTROLLED IN L3.
  - 6 DIMENSION b1, b3 APPLY TO BASE METAL ONLY.
  - 7 OUTLINE CONFORMS TO JEDEC OUTLINE TO-251AA.
  - 8 CONTROLLING DIMENSION : INCHES.

### LEAD ASSIGNMENTS

#### HEXFEET

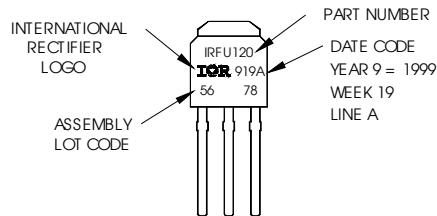
- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE
- 4.- DRAIN

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	2.18	2.39	0.086	0.094	
A1	0.89	1.14	0.035	0.045	
b	0.64	0.89	0.025	0.035	
b1	0.64	0.79	0.025	0.031	4
b2	0.76	1.14	0.030	0.045	
b3	0.76	1.04	0.030	0.041	
b4	5.00	5.46	0.195	0.215	4
c	0.46	0.61	0.018	0.024	
c1	0.41	0.56	0.016	0.022	
c2	0.46	0.86	0.018	0.035	
D	5.97	6.22	0.235	0.245	3, 4
D1	5.21	-	0.205	-	4
E	6.36	6.73	0.250	0.265	3, 4
E1	4.32	-	0.170	-	4
e	2.29		0.090 BSC		
L	8.89	9.60	0.350	0.380	
L1	1.91	2.29	0.075	0.090	
L2	0.89	1.27	0.035	0.050	
L3	1.14	1.52	0.045	0.060	5
ø1	0"	15'	0"	15'	

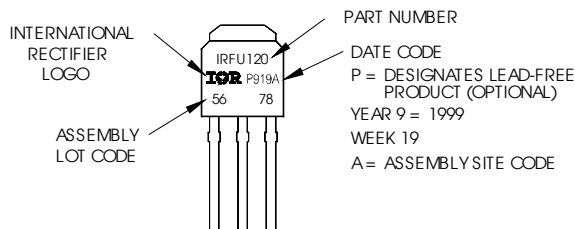
## I-Pak (TO-251AA) Part Marking Information

EXAMPLE: THIS IS AN IRFU120  
WITH ASSEMBLY  
LOT CODE 5678  
ASSEMBLED ON WW 19, 1999  
IN THE ASSEMBLY LINE "A"

Note: "P" in assembly line  
position indicates "Lead-Free"

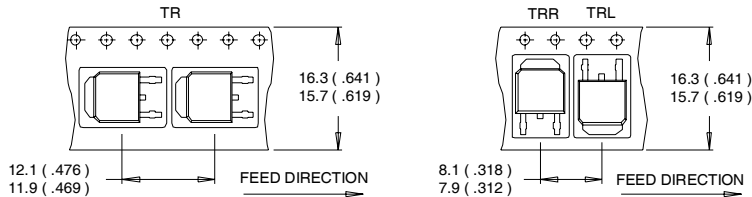


OR

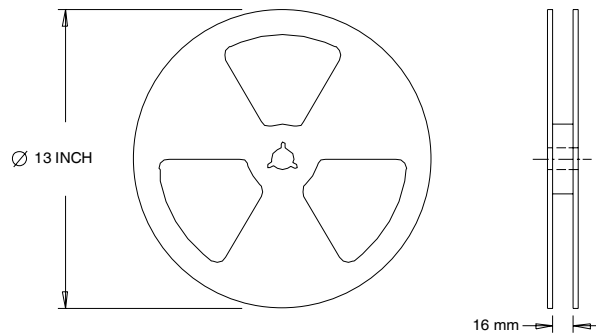


## D-Pak (TO-252AA) Tape & Reel Information

Dimensions are shown in millimeters (inches)



- NOTES:
1. CONTROLLING DIMENSION: MILLIMETER.
  2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS ( INCHES ).
  3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



- NOTES:
1. OUTLINE CONFORMS TO EIA-481.

### Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Limited by  $T_{Jmax}$ , starting  $T_J = 25^\circ\text{C}$ ,  $L = 0.55\text{mH}$ ,  $R_G = 25\Omega$ ,  $I_{AS} = 15\text{A}$ ,  $V_{GS} = 10\text{V}$
- ③  $I_{SD} \leq 25\text{A}$ ,  $di/dt \leq 290\text{A}/\mu\text{s}$ ,  $V_{DD} \leq V_{(BR)DSS}$ ,  $T_J \leq 175^\circ\text{C}$
- ④ Pulse width  $\leq 300\mu\text{s}$ ; duty cycle  $\leq 2\%$ .
- ⑤  $C_{OSS}$  eff. is a fixed capacitance that gives the same charging time as  $C_{OSS}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$ .
- ⑥ Limited by  $T_{Jmax}$ ; see Fig 12a, 12b, 15, 16 for typical repetitive avalanche performance.
- ⑦ This value determined from sample failure population. 100% tested to this value in production.

Data and specifications subject to change without notice.

This product has been designed and qualified for the Automotive [Q101]market.

Qualification Standards can be found on IR's Web site.

International  
**IR** Rectifier

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TAC Fax: (310) 252-7903

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